



HDP-1449 (Based on Form PTO-1449)

**PATENT AND TRADEMARK OFFICE  
INFORMATION DISCLOSURE CITATION**

(Use several sheets if necessary)

Sheet 1 of 1

ATTORNEY DOCKET NO.

SERIAL NO.

MP0357

10/627,269

APPLICANT

Chen, Hong-Yi Hubert et al

FILING DATE

GROUP

7/25/2003

2818

**U.S. PATENT DOCUMENTS**

Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
1.		5,970,241	10/19/1999	Deao, Douglas E. et al		
2.		6,279,101 B1	8/21/2001	Witt, David B. et al		
3.		5,497,499	3/5/1996	Garg, Sanjiv et al		
4.		5,560,032	9/24/1996	Nguyen, Le Trong et al		
5.		5,737,624	4/7/1998	Garg, Sanjiv et al		
6.		5,809,522	9/15/198	Novak, Steve et al		
7.		10/672,774		Hong-Yi Chen et al		9/26/2003

**FOREIGN PATENT DOCUMENTS**

Ref. Desig.	Examiner's Initials	Document Number	Date	Country	Class/ Subclass	Translation Yes	No
1.							

**OTHER DOCUMENTS (including Author, Title, Date, Pertinent Pages, etc.)**

Ref. Desig.	Examiner's Initials	
1.		Computer Architecture A Quantitative Approach, Second Edition, David A. Patterson and John L. Hennessy with a contribution by David Goldberg; 1996; 14 pages
2.		Superscalar Microprocessor Design; Miek Johnson, 1991; 3 pages
3.		MP0367 - Application entitled "Data Processing System with Partial Bypass Reorder Buffer and Combined Load/Store Arithmetic Logic Unit and Processing Method Thereof", Hong-Yi Chen et al; 9/26/2003; 58 pages

Examiner: /Hetul Patel/

Date Considered:

02/15/2008

EXAMINER: Please initial if citation considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /HBP/